Dustin Richmond – Curriculum Vitae

Email: drichmond@ucsc.edu Website: dustinrichmond.com

Research Interests

Computer architecture, reconfigurable and flexible systems; hardware design, languages, abstractions, and libraries; hardware security, side-channel mitigation, fingerprinting, and counterfeit detection.

Education

University of California, San Diego (UC San Diego) August 2012 - July 2018
Doctor of Philosophy in Computer Engineering
Master of Science in Computer Engineering

University of Washington (UW), Seattle September 2008 - June 2012
Bachelor of Science, *cum laude*, in Computer Engineering
Bachelor of Science, *cum laude*, in Electrical Engineering

Professional Appointments

Assistant Professor, University of California, Santa Cruz July 2022 - Present
- Taught undergraduate and graduate general education courses in the Department of Computer Science and Engingeering
- Optimized information side-channels to detect and classify hardware circuits [2, 4, 5, 6].

Postdoctoral Research Associate, University of Washington, Seattle September 2018 - July 2022
- A leading role in the development of HammerBlade, a DARPA-funded project (FA8650-18-2-7863).
- Investigated runtimes for efficient computation on heterogeneous manycore systems [3, 18, 9, 20].
- Emulated, simulated, and taped-out two manycore chips (GlobalFoundries 12 nm) [1, 7, 8].

Graduate Student Research Assistant, University of California, San Diego August 2012 - July 2018
- Thesis: Hardware Development for Non-Hardware Engineers [10, 11, 14].
- Developed RIFFA and PYNQ frameworks for deploying domain accelerators on FPGAs and Python-like language abstractions for enabling new users [21, 23].
- Built tools for creating high-quality 3D models of culturally significant *in situ* artifacts at excavation sites in Guatemala [22].

Visiting Scholar, Xilinx, Inc. May 2017 - December 2017
- Developed PYNQ, a library for reconfigurable systems; Ported PYNQ from Zynq to Zynq Ultrascale+; contributed PYNQ Overlays, tutorials, and libraries [10, 11].

Future Architectures and Systems Intern, Altera Corporation June 2013 - December 2013
- Evaluated the impact of proposed architectural (Routing, Hard IP Placement) and algorithmic changes for next generation chips and development tools using the Altera toolchain [14].

Notebook Chip Solutions Intern, NVIDIA Corporation June 2011 - September 2011
- Verified software, firmware, and hardware for the pre-production sign-off process for Fermi and Kepler using temperature control chambers, stress-testing suites, and high-frequency oscilloscopes.

Nanotechnology Researcher, Washington Technology Center August 2009 - September 2010
- Conducted experiments to develop and quantify the efficiency improvements of single-crystal thin film solar cells with nanoimprinted diffraction gratings in a class 100 cleanroom [24, 25].

Fellowships

2014-2016	Achievement Rewards for College Scientists (ARCS) Fellowship, San Diego Chapter
2012-2014	Charles Lee Powell Fellowship, UC San Diego
2012-2015	National Science Foundation Graduate Research Fellowship

Honors & Awards

2018	Excellence in Service and Leadership, UC San Diego Computer Science and Engineering
2016	Outstanding Community Leader, UC San Diego Graduate Student Association
2016	Best Social Hour Theme: Lock-picking, UC San Diego Computer Science and Engineering
2015	Travel Grant, NSF Early-Career Investigators Workshop on Cyber-Physical Systems
2013	Community Best Paper Award, Intl. Conference on Field Programmable Logic
2012	Top 150 Graduating Seniors, UW
2012	Spirit of Community Award, UW Electrical Engineering
2011	1st Place, CSE 472 Final Project, UW Computer Science and Engineering
2009	Eta Kappa Nu Honor Society Inductee, UW Iota Upsilon Chapter
2008-2012	Dean's List, UW

Professional and Academic Service

2021-2022	Publicity Chair, Intl. Symposium on Field-Programmable Gate Arrays (FPGA)
2021-2022	Technical Program Committee, FPGA
2021	Platform Chair, Architectural Support for Programming Languages & Operating Systems
2019-2020	Publicity Chair, Intl. Conf. on Field-Programmable Custom Computing Machines (FCCM)
2020-2021	Technical Program Committee, FCCM
2019	Organizer, Workshop on Secure Custom Computing Machines at FCCM
2019	Postdoc Representative, ECE Student Advisory Council, UW
2017	Organizer, Workshop on Negotiation and Persuasion, UC San Diego CSE
2017	Triathlon Club Team Captain, UC San Diego
2015-2017	Chair, Faculty Candidate Interview Committee, UC San Diego CSE
2013-2016	Student Chair, Ph.D. Recruitment, UC San Diego CSE
2014-2015	Student Chair, Graduate Community Council, UC San Diego CSE
2014	Speaker, Graduate Division NSF Fellowship Panel, UC San Diego
2013-2016	Organizer, CSE Department NSF Fellowship Workshop, UC San Diego CSE
2010-2012	President, Eta Kappa Nu Honor Society, Iota Upsilon Chapter
2010-2012	Member, Student Advisory Committee to the Provost, UW
2009-2010	Events Coordinator, Eta Kappa Nu Honor Society, UW Iota Upsilon Chapter

Teaching Experience

Spring 2018 **Teaching Assistant, WES 207: Capstone Project**

- Developed new Jupyter/PYNQ-based curriculum for Masters-level Wireless Embedded Systems (WES) course, taught lab sessions, graded coursework

Winter 2018 **Teaching Assistant, WES 269: Hardware for Embedded Systems**

- Assisted students on Jupyter/PYNQ-based assignments and graded final projects

Spring 2013 **Lab Assistant, CSE 87: Introduction to Robotics**

- Taught introductory programming and robotics concepts to undergraduates using Python and MIT App Inventor in a lab setting

Students Supervised & Mentored

Name [Publications]	Year(s)	Degree, Institution	Employer/Institution
Lauren Choquer$^{\triangledown}$	2021	B.S., UW '21	SpaceX
Sripathi Muralitharan$^{\triangledown}$	2021	M.S., UW '21	Samba Nova
Olivia Weng$^{\blacktriangle\ddagger}$	2020-	*Degree in Progress*	Ph.D., UC San Diego
Colin Drewes$^{\triangledown\dagger}$ [4, 6]	2020-2022	B.S./M.S., UC San Diego	Ph.D, Stanford
Richard Appen$^{\triangledown}$ [4]	2020-2021	*Degree in Progress*	B.S., UC San Diego
Steven Harris$^{\triangledown\diamond}$ [4]	2020-2021	*Degree in Progress*	B.S., UC San Diego
Marcus Chow$^{\blacktriangle}$	2020-2021	*Degree in Progress*	Ph.D., UC Riverside
Winnie Wang$^{\triangledown\diamond}$ [4]	2020-2021	B.S., UC San Diego '21	*To Be Determined*
Lin Cheng$^{\blacktriangle}$ [18]	2019-	*Degree in Progress*	Ph.D., Cornell University
Sasha Krassovsky$^{\triangledown}$	2019-2020	B.S., UW '20	SingleStore
Scott Davidson$^{\blacktriangle}$ [7, 8, 19, 9]	2018-	*Degree in Progress*	Ph.D., UW
Paul Gao$^{\blacktriangle}$ [7, 8]	2018-	*Degree in Progress*	Ph.D., UW
Daniel Petrisko$^{\blacktriangle}$ [8]	2018-	*Degree in Progress*	Ph.D., UW
Dai Cheol Jung$^{\blacktriangle}$ [7]	2018-	*Degree in Progress*	Ph.D., UW
Max Ruttenberg$^{\blacktriangle}$ [3, 18]	2018-	*Degree in Progress*	Ph.D., UW
Aditya Kamath$^{\blacktriangle}$	2021-	*Degree in Progress*	Ph.D., UW
Bandhav Veluri$^{\blacktriangle}$ [18]	2018-2020	*Degree in Progress*	Ph.D., UW
Mara Kirdani-Ryan$^{\blacktriangle}$	2018-2019	*Degree in Progress*	Ph.D., UW
Emily Furst$^{\blacktriangle}$ [3]	2018-2021	Ph.D, UW '21	AMD Research
Borna Ehsani$^{\triangledown}$ [18]	2018-2020	M.S., UW '20	Apple
Leonard Xiang$^{\triangledown}$	2018-2020	M.S., UW '19	*To Be Determined*
Mustafa Gobulukoglu$^{\triangledown}$ [5, 6]	2018-2020	M.S., UC San Diego '20	Northrup Grumman
Katie Lim$^{\blacktriangle}$	2018-2019	*Degree in Progress*	Ph.D., UW
Sivasankar Palaniappan$^{\triangledown}$	2018-2019	M.S., UC San Diego '19	Siemens
Indira Avendano$^{\triangledown\cup}$ [10]	2018	*Degree in Progress*	B.S., University of Central Florida
Brennan Cain$^{\triangledown\cup}$ [10]	2018	*Degree in Progress*	B.S., University of South Carolina
Zain Merchant$^{\triangledown\cup}$ [10]	2018	B.S., U. Texas '18	NASA Langley
Kevin Thai$^{\triangledown}$ [16]	2016	B.S., UC San Diego '17	Research Assistant, UC San Diego
Dominique Meyer$^{\triangledown}$ [28]	2015-2016	B.S., UC San Diego '16	Ph.D., UC San Diego
Zachary Blair$^{\triangledown}$ [13]	2014-2015	M.S., UC San Diego '16	Xilinx/AMD
Antonella Wilby‡	2014-2015	B.S., UC San Diego '15	Ph.D., UC San Diego
Stephanie Conley$^{\triangledown\dagger}$	2014-2015	B.S., UC San Diego '15	Lab Manager, Stanford
Zachary Barnes$^{\triangledown}$ [28]	2014-2015	B.S., U. Pittsburgh '16	Bolt
Matthew Hogains$^{\triangledown}$ [23, 16]	2014-2016	B.S., UC San Diego '16	NWDA Labs
Sabrina Trinh$^{\triangledown\cup}$ [22, 28]	2014-2016	B.S., UC San Diego '16	General Atomics
David Dantas$^{\triangledown\cup}$ [28]	2014-2015	B.S., UC San Diego '16	CooperVision
Jeremy Blackstone$^{\triangledown\star\dagger}$ [16]	2014	Ph.D., UC San Diego '21	Asst. Professor, Howard University
Alexandria Shearer‡ [15]	2013-2016	M.S., UC San Diego '16	NASA JPL
Riley Yeakle†	2013-2016	M.S., UC San Diego '16	Apple
Alireza Khodamoradi†	2013-2015	Ph.D, UC San Diego '21	Xilinx/AMD
Perry Naughton‡ [22, 28]	2012-2013	Ph.D, UC San Diego '18	Toyon Corporation
Alric Althoff‡ [21]	2012-2013	Ph.D, UC San Diego '18	Tortuga Logic

▲: Supervised on doctorate-level research project
▽: Supervised on bachelor's or master's-level research project
∪: Mentored through NSF Research Experience for Undergraduates
◇: Mentored through UC San Diego Early Research Scholars Program (ERSP)
⋆: Mentored through Howard University + UC San Diego STARS Program
†: Assisted NSF Graduate Research Fellowship Application
‡: Assisted successful NSF Graduate Research Fellowship Application

Conference Publications (Peer Reviewed)

[1] L. Cheng*, M. Ruttenberg*, D. C. Jung, **D. Richmond**, M. Taylor, M. Oskin, and C. Batten. "Beyond Static Parallel Loops: Supporting Dynamic Task Parallelism on Manycore Architectures with Software-Manged Scratchpad Memories". In: *Architectural Support for Programming Languages and Operating Systems*. Vol. 3. ASPLOS '23. Vancouver, BC, Canada: Association for Computing Machinery, 2023.

[2] C. Drewes, O. Weng, K. Ryan, B. Hunter, C. McCarty, R. Kastner, and **D. Richmond**. "Turn on, Tune in, Listen up: Maximizing Side-Channel Recovery in Time-to-Digital Converters". In: *International Symposium on Field Programmable Gate Arrays*. FPGA '23. Monterey, CA, USA: Association for Computing Machinery, 2023, pp. 111–122. DOI: 10.1145/3543622.3573193.

[3] A. Brahmakshatriya, E. Furst, V. A. Ying, C. Hsu, C. Hong, M. Ruttenberg, Y. Zhang, D. C. Jung, **D. Richmond**, M. B. Taylor, J. Shun, M. Oskin, D. Sanchez, and S. Amarasinghe. "Taming the Zoo: The Unified GraphIt Compiler Framework for Novel Architectures". In: *International Symposium on Computer Architecture (ISCA)*. ISCA '21. ACM. 2021.

[4] C. Drewes, S. Harris, W. Wang, R. Appen, O. Weng, R. Kastner, W. Hunter, C. McCarty, and **D. Richmond**. "A Tunable Dual-Edge Time-to-Digital Converter". In: *International Symposium on Field-Programmable Custom Computing Machines (FCCM)*. FCCM '21. IEEE. 2021, pp. 1–1.

[5] M. Gobulukoglu, C. Drewes, B. Hunter, R. Kastner, and **D. Richmond**. "Classifying Computations on Multi-Tenant FPGAs". In: *International Symposium on Field-Programmable Gate Arrays (FPGA)*. FPGA '21. ACM/SIGDA. 2021, p. 227.

[6] M. Gobulukoglu, C. Drewes, B. Hunter, R. Kastner, and **D. Richmond**. "Classifying Computations on Multi-Tenant FPGAs". In: *Design Automation Conference (DAC)*. DAC '21. 2021.

[7] D. C. Jung, S. Davidson, C. Zhao, **D. Richmond**, and M. B. Taylor. "Ruche Networks: Wire-Maximal, No-Fuss NoCs". In: *International Symposium on Networks-on-Chip (NOCS)*. NOCS '20. IEEE/ACM. 2020, pp. 1–8.

[8] D. Petrisko, C. Zhao, S. Davidson, P. Gao, **D. Richmond**, and M. B. Taylor. "NoC Symbiosis". In: *International Symposium on Networks-on-Chip (NOCS)*. NOCS '20. IEEE/ACM. 2020, pp. 1–8.

[9] A. Rovinski, C. Zhao, K. Al-Hawaj, P. Gao, S. Xie, C. Torng, S. Davidson, A. Amarnath, L. Vega, B. Veluri, A. Rao, T. Ajayi, J. Puscar, S. Dai, R. Zhao, **D. Richmond**, Z. Zhang, I. Galton, C. Batten, M. Taylor, and R. Dreslinski. "A 1.4 GHz 695 Giga RISC-V Inst/s 496-Core Manycore Processor With Mesh On-Chip Network and an All-Digital Synthesized PLL in 16nm CMOS". In: *Symposium on VLSI Circuits (VLSI)*. IEEE. 2019, pp. C30–C31.

[10] B. Cain, Z. Merchant, I. Avendano, **D. Richmond**, and R. Kastner. "PynqCopter-An Open-source FPGA Overlay for UAVs". In: *International Conference on Big Data (Big Data)*. Big Data '18. IEEE. 2018, pp. 2491–2498.

[11] **D. Richmond**, M. Barrow, and R. Kastner. "Everyone's a Critic: A Tool for Exploring RISC-V Projects". In: *International Conference on Field Programmable Logic and Applications (FPL)*. FPL '18. IEEE. 2018, pp. 260–2604.

[12] D. Lee, A. Althoff, **D. Richmond**, and R. Kastner. "A Streaming Clustering Approach using a Heterogeneous System for Big Data Analysis". In: *International Conference on Computer-Aided Design (ICCAD)*. ICCAD '17. IEEE/ACM. 2017, pp. 699–706.

[13] J. Matai, **D. Richmond**, D. Lee, Z. Blair, Q. Wu, A. Abazari, and R. Kastner. "Resolve: Generation of High-Performance Sorting Architectures for High-level Synthesis". In: *International Symposium on Field-Programmable Gate Arrays (FPGA)*. FPGA '16. ACM/SIGDA. 2016, pp. 195–204.

[14] **D. Richmond**, J. Blackstone, M. Hogains, K. Thai, and R. Kastner. "Tinker: Generating Custom Memory Architectures for Altera's OpenCL Compiler". In: *International Symposium on Field-Programmable Custom Computing Machines (FCCM)*. FCCM '16. IEEE. 2016, pp. 21–24.

[15] Q. Gautier, A. Shearer, J. Matai, **D. Richmond**, P. Meng, and R. Kastner. "Real-time 3D Reconstruction for FPGAs: A Case Study for Evaluating the Performance, Area, and Programmability Trade-offs of the Altera OpenCL SDK". In: *International Conference on Field-Programmable Technology (FPT)*. FPT '14. IEEE. 2014, pp. 326–329.

[16] **D. Richmond**, R. Kastner, A. Irturk, and J. McGarry. "A FPGA Design for High-Speed Feature Extraction from a Compressed Measurement Stream". In: *International Conference on Field programmable Logic and Applications (FPL)*. FPL '13. IEEE. 2013, pp. 1–8.

[17] E. Brossard, **D. Richmond**, J. Green, C. Ebeling, L. Ruzzo, C. Olson, and S. Hauck. "A Model for Programming Data-Intensive Applications on FPGAs: A Genomics Case Study". In: *Symposium on Application Accelerators in High Performance Computing (SAAHPC)*. SAAHPC '12. IEEE. 2012, pp. 84–93.

Journal Publications (Peer Reviewed)

[18] L. Cheng, P. Pan, Z. Zhao, K. Ranjan, J. Weber, P. Ivanov, B. Veluri, S. B. Ehsani, M. Ruttenberg, D. Cheol Jung, **D. Richmond**, M. B. Taylor, Z. Zhang, and C. Batten. "A Tensor Processing Framework for CPU-Manycore Heterogeneous Systems". In: *Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)* (2021).

[19] M. B. Taylor, L. Vega, M. Khazraee, I. Magaki, S. Davidson, and **D. Richmond**. "ASIC Clouds: Specializing the Datacenter for Planet-Scale Applications". In: *Communications of the ACM (CACM)* 63 (2020), pp. 103–109.

[20] A. Rovinski, C. Zhao, K. Al-Hawaj, P. Gao, S. Xie, C. Torng, S. Davidson, A. Amarnath, L. Vega, B. Veluri, A. Rao, T. Ajayi, J. Puscar, S. Dai, R. Zhao, **D. Richmond**, Z. Zhang, I. Galton, C. Batten, M. Taylor, and R. Dreslinski. "Evaluating Celerity: A 16nm 695 Giga-RISC-V Instructions/s Manycore Processor with Synthesizable PLL". In: *Solid-State Circuits Letters* 2.12 (2019), pp. 289–292.

[21] **D. Richmond**, A. Althoff, and R. Kastner. "Synthesizable Higher-Order Functions for C++". In: *Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)* 37.11 (2018), pp. 2835–2844.

[22] T. G. Garrison, **D. Richmond**, P. Naughton, E. Lo, S. Trinh, Z. Barnes, A. Lin, C. Schurgers, R. Kastner, and S. E. Newman. "Tunnel Vision: documenting excavations in three dimensions with Lidar technology". In: *Advances in Archaeological Practice* 4.2 (2016), pp. 192–204.

[23] M. Jacobsen, **D. Richmond**, M. Hogains, and R. Kastner. "RIFFA 2.1: A Reusable Integration Framework for FPGA Accelerators". In: *Transactions on Reconfigurable Technology and Systems (TRETS)* 8.4 (2015).

[24] **D. Richmond**, Q. Zhang, G. Cao, and D. N. Weiss. "Pressureless nanoimprinting of anatase TiO_2 precursor films". In: *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena* 29.2 (2011).

[25] D. N. Weiss, B. G. Lee, **D. Richmond**, W. Nemeth, Q. Wang, D. A. Keszler, and H. M. Branz. "Diffractive light trapping in crystal-silicon films: experiment and electromagnetic modeling". In: *Applied Optics* 50.29 (2011), pp. 5728–5734.

Technical Reports

[26] **D. Richmond**, M. Jacobsen, and K. Ryan. *RIFFA 2.2.2 Documentation*. University of California, San Diego. San Diego, California, USA, 2016.

[27] **D. Richmond**, M. Jacobsen, and K. Ryan. *RIFFA 2.2.1 Documentation*. University of California, San Diego. San Diego, California, USA, 2015.

[28] S. Trinh, **D. Richmond**, P. Naughton, E. Lo, D. Dantas, D. Meyer, A. Lin, C. Schurgers, R. Kastner, and T. Garrison. *La documentación en 3D de excavaciones y artefactos arqueológicos*. Instituto de Antropología e Historia. Guatemala City, Guatemala, 2015.

[29] **D. Richmond**, M. Jacobsen, and K. Ryan. *RIFFA 2.2.0 Documentation*. University of California, San Diego. San Diego, California, USA, 2014.

Workshop Papers

[30] J. Matai, **D. Richmond**, D. Lee, and R. Kastner. *Enabling FPGAs for the Masses*. 2014.

MEDIA & PUBLICITY

[M1] "Promoting equity in engineering". In: *University of Washington College of Engineering Newsletter* (Nov. 15, 2021). https://www.engr.washington.edu/news/article/2021-11-15/promoting-equity-engineering/.

[M2] "Jeremy Blackstone (Ph.D.'21): Mountaineer, Explorer, and Howard Professor". In: *U.C. San Diego Computer Science and Engineering Newsletter* (May 22, 2021). https://cse.ucsd.edu/about/news/jeremy-blackstone-phd-21-mountaineer-explorer-and-howard-professor.

[M3] M. Ruttenberg and M. Taylor. *The HammerBlade RISC-V Manycore: A programmable, scalable RISC-V fabric*. https://archive.fosdem.org/2020/schedule/event/riscv_hammerblade/. Feb. 1, 2020.

[M4] B. Cain. *PYNQ-Copter Maiden Flight, August 2019*. https://www.youtube.com/watch?v=EVH-jH0RqAY. Aug. 18, 2018.

[M5] A. Williams. "Catching The (PCIe) Bus". In: *Hackaday* (Feb. 17, 2018). https://hackaday.com/2018/02/17/catching-the-pcie-bus/.

[M6] S. Leibson. "12 PYNQ Hackathon teams competed for 30 hours, inventing remote-controlled robots, image recognizers, and an air keyboard". In: *Xilinx XCell Daily Blog* (Oct. 8, 2017). https://forums.xilinx.com/t5/Xcell-Daily-Blog-Archived/12-PYNQ-Hackathon-teams-competed-for-30-hours-inventing-remote/ba-p/799208.

[M7] S. Leibson. "The 2017 PYNQ Hackathon: Pictures from a Competition. A Photo Essay." In: *Xilinx XCell Daily Blog* (Oct. 10, 2017). https://forums.xilinx.com/t5/Xcell-Daily-Blog-Archived/The-2017-PYNQ-Hackathon-Pictures-from-a-Competition-A-Photo/ba-p/799700.

[M8] "CSE Closes out Successful Hiring Season for 2016-2017". In: *U.C. San Diego Computer Science and Engineering Newsletter* (Aug. 18, 2017). https://cse.ucsd.edu/about/news/cse-closes-out-successful-hiring-season-2016-2017.

[M9] Q. Gautier. *Engineers for Exploration - Maya Archaeology*. https://www.youtube.com/watch?v=Ax6hLmHahLg. Oct. 12, 2016.

[M10] Q. Gautier. *UCSD Engineers for Exploration - Maya Archaeology Overview*. https://www.youtube.com/watch?v=7tKovc0Eo54. Oct. 12, 2016.

[M11] "NSF Graduate Research Fellowships to CSE Students". In: *U.C. San Diego Computer Science and Engineering Newsletter* (Feb. 4, 2015). https://www.calit2.net/newsroom/article.php?id=2556.

[M12] J. Stone. "Drones, Lasers Help Archaeologists Study Ancient Mayan Ruins Hidden In Guatemala Jungle". In: *International Business Times* (Sept. 17, 2014). https://www.ibtimes.com/drones-lasers-help-archaeologists-study-ancient-mayan-ruins-hidden-guatemala-jungle-video-1690757.

[M13] T. Fox. "Capturing Ancient Maya Sites from Both a Rat's and a "Bat's Eye View"". In: *California Institute for Telecommunications and Information Technology Newsletter* (Aug. 12, 2014). https://www.calit2.net/newsroom/article.php?id=2420.

[M14] C. Bishop. "Dancing with Drones: UW students and autonomous aircraft". In: *Geekwire* (Mar. 12, 2011). https://www.geekwire.com/2011/dancing-drones-uw-students-autonomous-aircraft/.

[M15] K. Long. "Class Projects get Flight Test". In: *Seattle Times* (Mar. 12, 2011). http://lazowska.cs.washington.edu/seattle.times.quad.jpg.

[M16] C. Woodward. "Quadricopters Take Over UW's Allen Center". In: *Xconomy* (Mar. 12, 2011). https://www.xconomy.com/seattle/2011/03/07/quadricopters-take-over-uws-allen-center-atrium-for-electrical-engineering-class-demo/.

Invited Presentations

- "Optimizing Architectures with Ruche Networks," Semiconductor Research Corporation (SRC) Applications Driving Architectures (ADA) Liason Meeting, Virtual, 2021
- "NoC Symbiosis: 10x More Bandwidth for Network-on-Chips," SRC ADA Center e-Workshop, Virtual, 2021
- "NSF Graduate Research Fellowship Process, Explained," Engineers for Exploration Research Experience for Undergraduates Site, San Diego, California, 2020
- "Deploying Sensors in the Datacenter," Workshop on Secure Custom Computing Machines at International Conference on Field-Programmable Custom Computing Machines, San Diego, California, 2019
- "NSF Graduate Research Fellowship Process, Explained," Engineers for Exploration Research Experience for Undergraduates Site, San Diego, California, 2018
- "Using FPGAs, Safely," Research Talk, University of Texas at Austin, 2018
- "Using FPGAs, Safely," Research Talk, University of California, Santa Barbara, 2018
- "Platforms (And Usability)," Fast Start Workshop at International Conference on Field-Programmable Custom Computing Machines, Washington, D.C., 2016
- "Building Heterogeneous Systems Using RIFFA and Trellis" Lawrence Berkeley National Laboratory, Berkeley, California 2014
- "Building Heterogeneous Systems Using RIFFA and Trellis" Research Talk at Microsoft Research, Seattle, Washington, 2014

Conference Presentations

- "NoC Symbiosis," International Symposium on Networks-on-Chip, Virtual, 2020 `https://www.youtube.com/watch?v=bbe0RCti_CM`
- "Synthesizable Higher-Order functions for C++," International Conference on Hardware/Software Codesign and System Synthesis, Turin, Italy, 2018
- "Tinker: Generating Custom Memory Architectures for Altera's OpenCL Compiler," International Conference on Field-Programmable Custom Computing Machines, Washington D.C., 2016
- "A FPGA Design for High Speed Feature Extraction From a Compressed Measurement Stream," International Conference on Field Programmable Logic, Porto, Portugal, 2013

Posters

- "HammerBlade: Overcoming Overspecialization with Software-Defined Hardware," DARPA Microsystems Technology Office Electronics Resurgence Initiative Summit, Detroit, Michigan, 2021
- "HammerBlade: Continuous Synthesis of Polymorphic Hardware/Software," DARPA Microsystems Technology Office Electronics Resurgence Initiative Summit, Detroit, Michigan, 2019
- "Synthesizable Higher-Order functions for C++," International Conference on Hardware/Software Codesign and System Synthesis, Turin, Italy 2018
- "Tinker: Generating Custom Memory Architectures for Altera's OpenCL Compiler," International Conference on Field-Programmable Custom Computing Machines, Washington, D.C., 2016
- "Using Computer Vision to Map Environments for Archeological Documentation," University of California, San Diego Research Expo, San Diego, California, 2015
- "Using Efficient Heterogeneous Systems in Smart Cities," 2015 NSF Early-Career Investigators (ECI) Workshop on Smart City and Cyber-Physical Systems, Seattle, Washington, 2015
- "Trellis: A Framework for Heterogeneous Desktop Supercomputers," University of California, San Diego Research Expo, San Diego, California, 2014
- "Design of an Ultra High-Speed Active 3D Scanner," University of California, San Diego Research Expo, San Diego, California, 2013