Dustin Alexander Richmond

Email: dustinar@uw.edu Website: dustinrichmond.com

Education

University of California, San Diego August 2012 - July 2018
Doctor of Philosophy in Computer Engineering
Master of Science in Computer Engineering

University of Washington, Seattle September 2008 - June 2012
Bachelor of Science in Computer Engineering
Bachelor of Science in Electrical Engineering

Employment

Postdoctoral Scholar, University of Washington, Seattle September 2018 - Present

- A leading role in a DARPA-funded project, HammerBlade: A Supercomputer for ML and Graphs (FA8650-18-2-7863).
- Investigated runtimes for efficient computation on heterogeneous manycore systems [1, 16, 7, 18].
- Emulated, simulated, and taped-out (GlobalFoundries 14nm) a heterogeneous manycore chip [5, 6].
- Optimized information side-channels to detect and classify hardware circuits [2, 3, 4].

Graduate Student Research Assistant, University of California, San Diego August 2012 - July 2018

- Thesis: A Software-Like Environment for Field Programmable Gate Arrays [8, 19, 9, 12, 21]
- Built research tools for capturing high-quality 3D models of culturally significant *in situ* artifacts at excavation sites in Guatemala [20].

Visiting Scholar / PYNQ Intern, Xilinx, Inc. May 2017 - December 2017

- Developed PYNQ, a library for reconfigurable systems; Ported PYNQ from Zynq to Zynq Ultrascale+; contributed PYNQ Overlays, tutorials, and libraries [8, 9].

Future Architectures and Systems Intern, Altera Corporation June 2013 - December 2013

- Evaluated the impact of proposed architectural (Routing, Hard IP Placement) and algorithmic changes for next generation chips and development tools using the Altera toolchain [12].

Notebook Chip Solutions Intern, NVIDIA Corporation June 2011 - September 2011

- Verified software, firmware, and hardware as part of the pre-production verification process during Fermi/Kepler bringup using temperature-controlled stress-testing suites and high-frequency oscilloscopes.

Nanotechnology Researcher, Washington Technology Center August 2009 - September 2010

- Conducted experiments to develop and quantify the efficiency improvements of single-crystal thin film solar cells with nanoimprinted diffraction gratings in a class 100 cleanroom [22, 23].

Fellowships

2014-2016	Achievement Rewards for College Scientists (ARCS) Fellowship, San Diego Chapter
2012-2014	Charles Lee Powell Fellowship, University of California, San Diego
2012-2015	National Science Foundation Graduate Research Fellowship

Awards

2018	Award for Excellence in Leadership, Dept. of Computer Science and Engineering
2016	Outstanding Community Leader Award, Graduate Student Association
2013	Community Best Paper Award, Intl. Conference on Field Programmable Logic
2012	Top 150 Graduating Seniors, University of Washington
2012	Spirit of Community Award, Department of Electrical Engineering
2009	Eta Kappa Nu Honor Society Inductee, Iota Upsilon Chapter
2008-2012	Dean's List, University of Washington

Service

2021-2022	Publicity Chair, Intl. Symposium on Field-Programmable Gate Arrays (FPGA)
2021-2022	Technical Program Committee, FPGA
2021	Platform Chair, Intl. Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS)
2019-2020	Publicity Chair, Intl. Conf. on Field-Programmable Custom Computing Machines (FCCM)
2020-2021	Technical Program Committee, FCCM
2019	Organizer, Workshop on Secure Custom Computing Machines at FCCM
2015-2017	Chair, Faculty Candidate Interview Committee, University of California, San Diego
2013-2016	Student Chair, PhD Recruitment, University of California, San Diego
2014-2015	Student Chair, Graduate Community Council, University of California, San Diego
2013-2016	Organizer, NSF Fellowship Panel, University of California, San Diego
2010-2012	President, Eta Kappa Nu Honor Society, Iota Upsilon Chapter
2010-2012	Member, Student Advisory Committee to the Provost, University of Washington
2009-2010	Events Coordinator, Eta Kappa Nu Honor Society, Iota Upsilon Chapter

Teaching

Spring 2018 **Teaching Assistant, WES 207: Capstone Project**

- Developed new Jupyter/PYNQ-based curriculum for Masters-level Wireless Embedded Systems (WES) course, lectured lab sessions, graded coursework

Winter 2018 **Teaching Assistant, WES 269: Hardware for Embedded Systems**

- Assisted students with Wireless Embedded Systems capstone projects, graded final presentations and projects

Spring 2013 **Lab Assistant, CSE 87: Introduction to Robotics**

- Taught introductory programming and robotics concepts to undergraduates using Python and MIT App Inventor in a lab setting

Undergraduate Research Mentorship

2018-	HammerBlade: Synthesis of Polymorphic Software, University of Washington[16]
2018-	FPGA Hardware Security, University of Washington[2, 3, 4]
2013-2018	NSF Research Experience for Undergraduates, University of California, San Diego[8, 20, 26]
2013-2018	Engineers for Exploration, University of California, San Diego[20, 26]

Project Websites

- HammerBlade - Continuous Synthesis of Polymorphic Hardware/Software `github.com/bespoke-silicon-group/bsg_bladerunner`
- RIFFA - A Reusable Integration Interface for FPGA Accelerators - `github.com/kastnerrg/riffa`
- Documenting Cultural Heritage in Guatemala - `e4e.ucsd.edu/maya-archaeology`
- Engineers for Exploration - `http://e4e.ucsd.edu/`

Conference Publications (Peer Reviewed)

[1] A. Brahmakshatriya, E. Furst, V. A. Ying, C. Hsu, C. Hong, M. Ruttenberg, Y. Zhang, D. C. Jung, **D. Richmond**, M. B. Taylor, J. Shun, M. Oskin, D. Sanchez, and S. Amarasinghe. "Taming the Zoo: The Unified GraphIt Compiler Framework for Novel Architectures". In: *International Symposium on Computer Architecture (ISCA)*. ISCA '21. ACM. 2021.

[2] C. Drewes, S. Harris, W. Wang, R. Appen, O. Weng, R. Kastner, W. Hunter, C. McCarty, and **D. Richmond**. "A Tunable Dual-Edge Time-to-Digital Converter". In: *International Symposium on Field-Programmable Custom Computing Machines (FCCM)*. FCCM '21. IEEE. 2021, pp. 1–1.

[3] M. Gobulukoglu, C. Drewes, B. Hunter, R. Kastner, and **D. Richmond**. "Classifying Computations on Multi-Tenant FPGAs". In: *International Symposium on Field-Programmable Gate Arrays (FPGA)*. FPGA '21. ACM/SIGDA. 2021, p. 227.

[4] M. Gobulukoglu, C. Drewes, B. Hunter, R. Kastner, and **D. Richmond**. "Classifying Computations on Multi-Tenant FPGAs". In: *Design Automation Conference (DAC)*. DAC '21. 2021.

[5] D. C. Jung, S. Davidson, C. Zhao, **D. Richmond**, and M. B. Taylor. "Ruche Networks: Wire-Maximal, No-Fuss NoCs". In: *International Symposium on Networks-on-Chip (NOCS)*. NOCS '20. IEEE/ACM. 2020, pp. 1–8.

[6] D. Petrisko, C. Zhao, S. Davidson, P. Gao, **D. Richmond**, and M. B. Taylor. "NoC Symbiosis". In: *International Symposium on Networks-on-Chip (NOCS)*. NOCS '20. IEEE/ACM. 2020, pp. 1–8.

[7] A. Rovinski, C. Zhao, K. Al-Hawaj, P. Gao, S. Xie, C. Torng, S. Davidson, A. Amarnath, L. Vega, B. Veluri, A. Rao, T. Ajayi, J. Puscar, S. Dai, R. Zhao, **D. Richmond**, Z. Zhang, I. Galton, C. Batten, M. Taylor, and R. Dreslinski. "A 1.4 GHz 695 Giga RISC-V Inst/s 496-Core Manycore Processor With Mesh On-Chip Network and an All-Digital Synthesized PLL in 16nm CMOS". In: *Symposium on VLSI Circuits (VLSI)*. IEEE. 2019, pp. C30–C31.

[8] B. Cain, Z. Merchant, I. Avendano, **D. Richmond**, and R. Kastner. "PynqCopter-An Open-source FPGA Overlay for UAVs". In: *International Conference on Big Data (Big Data)*. Big Data '18. IEEE. 2018, pp. 2491–2498.

[9] **D. Richmond**, M. Barrow, and R. Kastner. "Everyone's a Critic: A Tool for Exploring RISC-V Projects". In: *International Conference on Field Programmable Logic and Applications (FPL)*. FPL '18. IEEE. 2018, pp. 260–2604.

[10] D. Lee, A. Althoff, **D. Richmond**, and R. Kastner. "A Streaming Clustering Approach using a Heterogeneous System for Big Data Analysis". In: *International Conference on Computer-Aided Design (ICCAD)*. ICCAD '17. IEEE/ACM. 2017, pp. 699–706.

[11] J. Matai, **D. Richmond**, D. Lee, Z. Blair, Q. Wu, A. Abazari, and R. Kastner. "Resolve: Generation of High-Performance Sorting Architectures for High-level Synthesis". In: *International Symposium on Field-Programmable Gate Arrays (FPGA)*. FPGA '16. ACM/SIGDA. 2016, pp. 195–204.

[12] **D. Richmond**, J. Blackstone, M. Hogains, K. Thai, and R. Kastner. "Tinker: Generating Custom Memory Architectures for Altera's OpenCL Compiler". In: *International Symposium on Field-Programmable Custom Computing Machines (FCCM)*. FCCM '16. IEEE. 2016, pp. 21–24.

[13] Q. Gautier, A. Shearer, J. Matai, **D. Richmond**, P. Meng, and R. Kastner. "Real-time 3D Reconstruction for FPGAs: A Case Study for Evaluating the Performance, Area, and Programmability Trade-offs of the Altera OpenCL SDK". In: *International Conference on Field-Programmable Technology (FPT)*. FPT '14. IEEE. 2014, pp. 326–329.

[14] **D. Richmond**, R. Kastner, A. Irturk, and J. McGarry. "A FPGA Design for High-Speed Feature Extraction from a Compressed Measurement Stream". In: *International Conference on Field programmable Logic and Applications (FPL)*. FPL '13. IEEE. 2013, pp. 1–8.

[15] E. Brossard, **D. Richmond**, J. Green, C. Ebeling, L. Ruzzo, C. Olson, and S. Hauck. "A Model for Programming Data-Intensive Applications on FPGAs: A Genomics Case Study". In: *Symposium on Application Accelerators in High Performance Computing (SAAHPC)*. SAAHPC '12. IEEE. 2012, pp. 84–93.

Journal Publications (Peer Reviewed)

[16] L. Cheng, P. Pan, Z. Zhao, K. Ranjan, J. Weber, P. Ivanov, B. Veluri, M. Ruttenberg, D. Cheol Jung, **D. Richmond**, M. B. Taylor, Z. Zhang, and C. Batten. "A Tensor Processing Framework for CPU-Manycore Heterogeneous Systems". In: *Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)* (2021).

[17] M. B. Taylor, L. Vega, M. Khazraee, I. Magaki, S. Davidson, and **D. Richmond**. "ASIC Clouds: Specializing the Datacenter for Planet-Scale Applications". In: *Communications of the ACM (CACM)* 63 (2020), pp. 103–109.

[18] A. Rovinski, C. Zhao, K. Al-Hawaj, P. Gao, S. Xie, C. Torng, S. Davidson, A. Amarnath, L. Vega, B. Veluri, A. Rao, T. Ajayi, J. Puscar, S. Dai, R. Zhao, **D. Richmond**, Z. Zhang, I. Galton, C. Batten, M. Taylor, and R. Dreslinski. "Evaluating Celerity: A 16nm 695 Giga-RISC-V Instructions/s Manycore Processor with Synthesizable PLL". In: *Solid-State Circuits Letters* 2.12 (2019), pp. 289–292.

[19] **D. Richmond**, A. Althoff, and R. Kastner. "Synthesizable Higher-Order Functions for C++". In: *Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)* 37.11 (2018), pp. 2835–2844.

[20] T. G. Garrison, **D. Richmond**, P. Naughton, E. Lo, S. Trinh, Z. Barnes, A. Lin, C. Schurgers, R. Kastner, and S. E. Newman. "Tunnel Vision: documenting excavations in three dimensions with Lidar technology". In: *Advances in Archaeological Practice* 4.2 (2016), pp. 192–204.

[21] M. Jacobsen, **D. Richmond**, M. Hogains, and R. Kastner. "RIFFA 2.1: A Reusable Integration Framework for FPGA Accelerators". In: *Transactions on Reconfigurable Technology and Systems (TRETS)* 8.4 (2015).

[22] **D. Richmond**, Q. Zhang, G. Cao, and D. N. Weiss. "Pressureless nanoimprinting of anatase TiO_2 precursor films". In: *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena* 29.2 (2011).

[23] D. N. Weiss, B. G. Lee, **D. Richmond**, W. Nemeth, Q. Wang, D. A. Keszler, and H. M. Branz. "Diffractive light trapping in crystal-silicon films: experiment and electromagnetic modeling". In: *Applied Optics* 50.29 (2011), pp. 5728–5734.

Technical Reports

[24] **D. Richmond**, M. Jacobsen, and K. Ryan. *RIFFA 2.2.2 Documentation*. University of California, San Diego. San Diego, California, USA, 2016.

[25] **D. Richmond**, M. Jacobsen, and K. Ryan. *RIFFA 2.2.1 Documentation*. University of California, San Diego. San Diego, California, USA, 2015.

[26] S. Trinh, **D. Richmond**, P. Naughton, E. Lo, D. Dantas, D. Meyer, A. Lin, C. Schurgers, R. Kastner, and T. Garrison. *La documentación en 3D de excavaciones y artefactos arqueológicos*. Instituto de Antropología e Historia. Guatemala City, Guatemala, 2015.

[27] **D. Richmond**, M. Jacobsen, and K. Ryan. *RIFFA 2.2.0 Documentation*. University of California, San Diego. San Diego, California, USA, 2014.

Workshop Papers

[28] J. Matai, **D. Richmond**, D. Lee, and R. Kastner. *Enabling FPGAs for the Masses*. 2014.

Presentations

- "NoC Symbiosis: 10x More Bandwidth for Network-on-Chips," ADA Center e-Workshop, Virtual, 2021
- "NoC Symbiosis," International Symposium on Networks-on-Chip, Virtual, 2020 `https://www.youtube.com/watch?v=bbe0RCti_CM`
- "Deploying Sensors in the Datacenter," Workshop on Secure Custom Computing Machines at the International Conference on Field-Programmable Custom Computing Machines, San Diego, California, 2019
- "Synthesizable Higher-Order functions for C++," International Conference on Hardware/Software Codesign and System Synthesis, Turin, Italy, 2018
- "Using FPGAs, Safely," Research Talk, University of California, Santa Barbara and University of Texas at Austin, 2018
- "Tinker: Generating Custom Memory Architectures for Altera's OpenCL Compiler," The International Conference on Field-Programmable Custom Computing Machines, Washington D.C., 2016
- "Platforms (And Usability)," Fast Start Workshop at International Conference on Field-Programmable Custom Computing Machines, Washington, D.C., 2016
- "Building Heterogeneous Systems Using RIFFA and Trellis" Research Talk at Microsoft Research, Seattle, Washington, 2014
- "A FPGA Design for High Speed Feature Extraction From a Compressed Measurement Stream," International Conference on Field Programmable Logic, Porto, Portugal, 2013

Posters

- "HammerBlade: Continuous Synthesis of Polymorphic Hardware/Software," DARPA Microsystems Technology Office Electronics Resurgence Initiative Summit, Detroit, Michigan, 2019
- "Synthesizable Higher-Order functions for C++," The International Conference on Hardware/Software Codesign and System Synthesis, Turin, Italy 2018
- "Tinker: Generating Custom Memory Architectures for Altera's OpenCL Compiler," International Conference on Field-Programmable Custom Computing Machines, Washington, D.C., 2016
- "Using Computer Vision to Map Environments for Archeological Documentation," University of California, San Diego Research Expo, San Diego, California, 2015
- "Trellis: A Framework for Heterogeneous Desktop Supercomputers," University of California, San Diego Research Expo, San Diego, California, 2014
- "Design of an Ultra High-Speed Active 3D Scanner," University of California, San Diego Research Expo, San Diego, California, 2013