Dustin Richmond – Curriculum Vitae

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Research Interests

Computer architecture, reconfigurable and flexible systems; hardware design, languages, abstractions, and libraries; hardware security, side-channel mitigation, fingerprinting, and counterfeit detection.

Teaching Interests

Computer architecture education, hardware design, hardware design abstractions, hardware description languages; Computer security, hardware security.

Education

University of California, San Diego August 2012 - July 2018
Doctor of Philosophy in Computer Engineering
Master of Science in Computer Engineering

University of Washington, Seattle September 2008 - June 2012
Bachelor of Science, *cum laude*, in Computer Engineering
Bachelor of Science, *cum laude*, in Electrical Engineering

Professional Appointments

Assistant Professor, University of California, Santa Cruz July 2022 - Present

- Teach undergraduate and graduate general education courses in the Department of Computer Science and Engingeering.
- Conduct research into novel manycore architectures [C16, C19].
- Study information side channels in ICs, specifically focusing on device power and manufacturing characteristics [C13, C14, C15, C17].

Postdoctoral Research Associate, University of Washington, Seattle September 2018 - July 2022

- A leading role in the development of HammerBlade, a DARPA-funded project (FA8650-18-2-7863).
- Investigated runtimes for efficient computation on heterogeneous manycore systems [C9, J6, C12, J8].
- Emulated, simulated, and taped-out two manycore chips (GlobalFoundries 12 nm) [C10, C11].

Graduate Student Research Assistant, University of California, San Diego August 2012 - July 2018

- Thesis: Hardware Development for Non-Hardware Engineers [C5, C7, C8].
- Developed RIFFA and PYNQ frameworks for deploying domain accelerators on FPGAs and Python-like language abstractions for enabling new users [J3, J5].
- Built tools for creating high-quality 3D models of culturally significant *in situ* artifacts at excavation sites in Guatemala [J4].

Visiting Scholar, Xilinx, Inc. May 2017 - December 2017

- Developed PYNQ, a library for reconfigurable systems; Ported PYNQ from Zynq to Zynq Ultrascale+; contributed PYNQ Overlays, tutorials, and libraries [C7, C8].

Future Architectures and Systems Intern, Altera Corporation June 2013 - December 2013

- Evaluated the impact of proposed architectural (Routing, Hard IP Placement) and algorithmic changes for next generation chips and development tools using the Altera toolchain [C5].

Notebook Chip Solutions Intern, NVIDIA Corporation June 2011 - September 2011
- Verified software, firmware, and hardware for the pre-production sign-off process for Fermi and Kepler using temperature control chambers, stress-testing suites, and high-frequency oscilloscopes.

Nanotechnology Researcher, Washington Technology Center August 2009 - September 2010
- Conducted experiments to develop and quantify the efficiency improvements of single-crystal thin film solar cells with nanoimprinted diffraction gratings in a class 100 cleanroom [J1, J2].

Fellowships

2014-2016	Achievement Rewards for College Scientists (ARCS) Fellowship, San Diego Chapter
2012-2014	Charles Lee Powell Fellowship, UC San Diego
2012-2015	National Science Foundation Graduate Research Fellowship

Honors and Awards

2023	Best Paper Nominee, ACM/SIGDA International Conference on Field Programmable Gate Arrays
2018	Excellence in Service and Leadership, UC San Diego Computer Science and Engineering
2016	Outstanding Community Leader, UC San Diego Graduate Student Association
2016	Best Social Hour Theme: Lock-picking, UC San Diego Computer Science and Engineering
2013	Community Best Paper Award, IEEE International Conference on Field Programmable Logic
2012	Cum Laude, University of Washington
2012	Top 150 Graduating Seniors, University of Washington
2012	Spirit of Community Award, University of Washington Electrical Engineering
2011	Best CSE 472 Final Project, University of Washington Computer Science and Engineering
2009	Eta Kappa Nu Honor Society Inductee, University of Washington Iota Upsilon Chapter
2008-2012	Dean's List, University of Washington

Grants and Donations

G1	2015	Travel Grant, NSF Early-Career Investigators Workshop on Cyber-Physical Systems ($1,500)
G2	2018	Co-Principal Investigator, AWS Cloud Credits for Research ($10,000)
G3	2022	Principal Investigator, Committee on Research Faculty Allowance ($2,000)
G4	2022	Co-Principal Investigator, AWS Cloud Credits for Research ($110,000)
G5	2023	Principal Investigator, Committee on Research Faculty Allowance ($2,000)
G6	2023	Principal Investigator, Xilinx Corporation, Hardware Donation ($500)
G7	2023	Principal Investigator, Intel Corporation, Hardware Donation ($1,000)
G8	2023	Principal Investigator, Intel Corporation, Hardware Donation ($9,500)
G9	2024	Principal Investigator, Committee on Research Faculty Allowance ($2,000)
G10	2024	*Repurposing DRAM for Neuromorphic Computation*, Principal Investigator, Committee on Research Large Grants Program ($12,000)
G11	2024	*Collaborative Research: SaTC: CORE: Medium: Pentimenti - Securing Cloud FPGAs from Analog Temporal Side Channels*, Principal Investigator ($1.2M)

University Service and Activities

Department Service

2020	Peer Reviewer, Pre-Application Review Service (PARS), University of Washington Paul G. Allen School of Computer Science and Engineering
2019	Postdoctoral Representative, Student Advisory Council, University of Washington Department of Electrical and Computer Engineering
2017	Organizer, Workshop on Negotiation and Persuasion, University of California San Diego Computer Science and Engineering
2015-2017	Chair, Faculty Candidate Interview Committee, University of California San Diego Computer Science and Engineering
2013-2016	Student Chair, Ph.D. Recruitment, University of California San Diego Computer Science and Engineering
2014-2015	Student Chair, Graduate Community Council, University of California San Diego Computer Science and Engineering
2013-2016	Organizer, NSF Fellowship Workshop, University of California San Diego Computer Science and Engineering
2012, 2009	Engineering Discovery Days, University of Washington Electrical Engineering Department

University Service

2023-2024	Member, Student Success Committee, University of California Santa Cruz Computer Science and Engineering
2023	Chair, Graduate Student Recruitment Committee, University of California Santa Cruz Computer Science and Engineering
2014	Speaker, NSF Fellowship Panel, University of California San Diego Graduate Division
2010-2012	Member, Student Advisory Committee to the Provost, University of Washington

Professional Service and Activities

Service

2024-2025	Workshops and Tutorials Chair, ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)
2021-2023	Website and Publicity Chair, ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)
2023	Organizer, Workshop on Security for Custom Computing Machines at the ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)
2022	Organizer, Workshop on Security for Custom Computing Machines at the IEEE International Conference on Field-Programmable Custom Computing Machines (FCCM)
2021	Platform Chair, ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)
2019-2020	Publicity Chair, IEEE International Conference on Field-Programmable Custom Computing Machines (FCCM)
2019	Organizer, Workshop on Secure Custom Computing Machines at the IEEE International Conference on Field-Programmable Custom Computing Machines (FCCM)
2010-2012	President, Eta Kappa Nu Honor Society, Iota Upsilon Chapter
2009-2010	Events Coordinator, Eta Kappa Nu Honor Society, Iota Upsilon Chapter

Committees

2025	Technical Program Committee, ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)
2021-2025	Technical Program Committee, ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)
2020-2022	Technical Program Committee, IEEE International Conference on Field-Programmable Custom Computing Machines (FCCM)
2022	External Technical Reviewer, IEEE/ACM International Symposium on Microarchitecture (MICRO)
2015	Reviewer, ACM Transactions on Reconfigurable Technology and Systems (TRETS)
2013	Reviewer, IEEE Transactions on Biomedical Circuits and Systems (TBioCAS)

Teaching

Courses Taught

Sp'24, Wi'23 **CSE 125: Logic Design with Verilog, University of California, Santa Cruz**

- Verilog digital logic design with emphasis on ASIC and FPGA design. Redesigned course to use open source tools and low-cost iCEBreaker boards.

Fa'23, Sp'23 **CSE 293: Advanced Topics in Computer Engineering, University of California, Santa Cruz**

- Seminar on research topics in computer engineering. Surveyed modern and novel hardware description languages through paper readings, literature searches, and the development of novel assignments.

Courses Assisted

Sp'18 **WES 207: Capstone Project, University of California, San Diego**

- Developed new Jupyter/PYNQ-based curriculum for Masters-level Wireless Embedded Systems (WES) course, taught lab sessions, graded coursework

Wi'18 **WES 269: Hardware for Embedded Systems, University of California, San Diego**

- Assisted students on Jupyter/PYNQ-based assignments and graded final projects

Sp'13 **CSE 87: Introduction to Robotics, University of California, San Diego**

- Taught introductory programming and robotics concepts to undergraduates using Python and MIT App Inventor in a lab setting

Students Supervised & Mentored

Legend

▲: Supervised on doctorate-level research project
▽: Supervised on bachelor's or master's-level research project
∪: Mentored through NSF Research Experience for Undergraduates
⋄: Mentored through UC San Diego Early Research Scholars Program (ERSP)
⋆: Mentored through Howard University + UC San Diego STARS Program
†: Assisted NSF Graduate Research Fellowship Application
‡: Assisted successful NSF Graduate Research Fellowship Application

Current Mentees

Name [Publications]	Year(s)	Degree, Institution	Employer/Institution

Tyler Sheaves▲ [J9]	2022-	*Degree in Progress*	Ph.D., UC Santa Cruz
Ella Lehavi▲	2024-	*Degree in Progress*	Ph.D., UC Santa Cruz
Phillip Marlowe▲	2023-	*Degree in Progress*	M.S., UC Santa Cruz
Aditya Bedekar▲	2024-	*Degree in Progress*	M.S., UC Santa Cruz
Sean Li▽	2024-	*Degree in Progress*	M.S., UC Santa Cruz
Gary Mejia▽	2023-	*Degree in Progress*	M.S., UC Santa Cruz
Mitchell Tansey▽	2023-	*Degree in Progress*	M.S., UC Santa Cruz
Dylan Brown▽	2024-	*Degree in Progress*	M.S., UC Santa Cruz
Raphael Huang▽	2024-	*Degree in Progress*	B.S., UC Santa Cruz
Ryan Taylor▽	2024-	*Degree in Progress*	B.S., UC Santa Cruz
Mattiwos Belachew▽	2024-	*Degree in Progress*	B.S., UC Santa Cruz
Arshan Rashidi▽	2024-	*Degree in Progress*	B.S., UC Santa Cruz
Chad Baker▽	2024-	*Degree in Progress*	B.S., UC Santa Cruz
Christian Li▽	2022-	*Degree in Progress*	B.S., UC Santa Cruz
Nithin Duvvuru▽	2024-	*Degree in Progress*	B.S., UC Santa Cruz
Isaac Garibay▽	2024-	*Degree in Progress*	B.S., UC Santa Cruz
Jackson Friday▽	2024-	*Degree in Progress*	B.S., UC Santa Cruz
Andrew Barth-Yi▽	2024-	*Degree in Progress*	B.S., UC Santa Cruz

PAST MENTEES

Name [Publications]	**Year(s)**	**Degree, Institution**	**Employer/Institution**
Yifan Zou▽	2023-2024	B.S., UC Santa Cruz	
Edwin Rojas-Torres▽	2024	B.S., UC Santa Cruz	
Rian Borah▲	2022-2023	*Degree in Progress*	B.S., UC Santa Cruz
Lauren Choquer▽	2021	B.S., UW '21	SpaceX
Sripathi Muralitharan▽	2021	M.S., UW '21	Samba Nova
Olivia Weng▲‡ [C13, C17, J9, C18]	2020-2022	*Degree in Progress*	Ph.D., UC San Diego
Colin Drewes▽† [C13, C15, C17, J9, C18]	2020-2022	B.S./M.S., UC San Diego	Ph.D, Stanford
Richard Appen▽ [C13]	2020-2021	*Degree in Progress*	B.S., UC San Diego
Steven Harris▽◇ [C13]	2020-2021	*Degree in Progress*	B.S., UC San Diego
Marcus Chow▲	2020-2021	*Degree in Progress*	Ph.D., UC Riverside
Winnie Wang▽◇ [C13]	2020-2021	B.S., UC San Diego '21	
Lin Cheng▲ [J8, C16]	2019-2023	Ph.D., Cornell Univ.	Apple Inc.
Sasha Krassovsky▽	2019-2020	B.S., UW '20	SingleStore
Scott Davidson▲ [C9, C10, C11, J7]	2018-2022	*Degree in Progress*	Ph.D., UW
Paul Gao▲ [C10, C11]	2018-2022	*Degree in Progress*	Ph.D., UW
Daniel Petrisko▲ [C11]	2018-2022	*Degree in Progress*	Ph.D., UW
Dai Cheol Jung▲ [C10]	2018-2022	*Degree in Progress*	Ph.D., UW
Max Ruttenberg▲ [C12, J8, C16]	2018-2022	*Degree in Progress*	Ph.D., UW
Aditya Kamath▲	2021-2022	*Degree in Progress*	Ph.D., UW
Bandhav Veluri▲ [J8]	2018-2020	*Degree in Progress*	Ph.D., UW
Mara Kirdani-Ryan▲	2018-2019	*Degree in Progress*	Ph.D., UW
Emily Furst▲ [C12]	2018-2021	Ph.D, UW '21	AMD Research
Borna Ehsani▽ [J8]	2018-2020	M.S., UW '20	Apple
Leonard Xiang▽	2018-2020	M.S., UW '19	
Mustafa Gobulukoglu▽ [C14, C15]	2018-2020	M.S., UC San Diego '20	Northrup Grumman
Katie Lim▲	2018-2019	*Degree in Progress*	Ph.D., UW
Sivasankar Palaniappan▽	2018-2019	M.S., UC San Diego '19	Siemens
Indira Avendano▽∪ [C7]	2018	B.S., Univ. of C. Florida	
Brennan Cain▽∪ [C7]	2018	B.S., Univ. of S. Carolina	
Zain Merchant▽∪ [C7]	2018	B.S., U. Texas '18	NASA Langley

Kevin Thai$^{\triangledown}$ [C2]	2016	B.S., UC San Diego '17	General Atomics
Dominique Meyer$^{\triangledown}$ [R3]	2015-2016	B.S., UC San Diego '16	Ph.D., UC San Diego
Zachary Blair$^{\triangledown}$ [C4]	2014-2015	M.S., UC San Diego '16	Xilinx/AMD
Antonella Wilby‡	2014-2015	B.S., UC San Diego '15	Ph.D., UC San Diego
Stephanie Conley$^{\triangledown\dagger}$	2014-2015	B.S., UC San Diego '15	Lab Manager, Stanford
Zachary Barnes$^{\triangledown}$ [R3]	2014-2015	B.S., U. Pittsburgh '16	Bolt
Matthew Hogains$^{\triangledown}$ [C2, J3]	2014-2016	B.S., UC San Diego '16	NWDA Labs
Sabrina Trinh$^{\triangledown\cup}$ [R3, J4]	2014-2016	B.S., UC San Diego '16	General Atomics
David Dantas$^{\triangledown\cup}$ [R3]	2014-2015	B.S., UC San Diego '16	CooperVision
Jeremy Blackstone$^{\triangledown\star\dagger}$ [C2]	2014	Ph.D., UC San Diego '21	Asst. Professor
Alexandria Shearer‡ [C3]	2013-2016	M.S., UC San Diego '16	NASA JPL
Riley Yeakle†	2013-2016	M.S., UC San Diego '16	Apple
Alireza Khodamoradi†	2013-2015	Ph.D, UC San Diego '21	Xilinx/AMD
Perry Naughton‡ [R3, J4]	2012-2013	Ph.D, UC San Diego '18	Toyon Corporation
Alric Althoff‡ [J5]	2012-2013	Ph.D, UC San Diego '18	ARM Research

Scholarly and Creative Work

Conference Publications (Peer Reviewed)

[C1] E. Brossard, **D. Richmond**, J. Green, C. Ebeling, L. Ruzzo, C. Olson, and S. Hauck. "A Model for Programming Data-Intensive Applications on FPGAs: A Genomics Case Study". In: *Symposium on Application Accelerators in High Performance Computing*. SAAHPC '12. IEEE. 2012, pp. 84–93. DOI: 10.1109/SAAHPC.2012.18.

[C2] **D. Richmond**, R. Kastner, A. Irturk, and J. McGarry. "A FPGA Design for High-Speed Feature Extraction from a Compressed Measurement Stream". In: *International Conference on Field programmable Logic and Applications*. FPL '13. IEEE. 2013, pp. 1–8. DOI: 10.1109/FPL.2013.6645527.

[C3] Q. Gautier, A. Shearer, J. Matai, **D. Richmond**, P. Meng, and R. Kastner. "Real-time 3D Reconstruction for FPGAs: A Case Study for Evaluating the Performance, Area, and Programmability Trade-offs of the Altera OpenCL SDK". In: *International Conference on Field-Programmable Technology*. FPT '14. IEEE. 2014, pp. 326–329. DOI: 10.1109/FPT.2014.7082810.

[C4] J. Matai, **D. Richmond**, D. Lee, Z. Blair, Q. Wu, A. Abazari, and R. Kastner. "Resolve: Generation of High-Performance Sorting Architectures for High-level Synthesis". In: *International Symposium on Field-Programmable Gate Arrays*. FPGA '16. ACM/SIGDA. 2016, pp. 195–204. DOI: 10.1145/2847263.2847268.

[C5] **D. Richmond**, J. Blackstone, M. Hogains, K. Thai, and R. Kastner. "Tinker: Generating Custom Memory Architectures for Altera's OpenCL Compiler". In: *International Symposium on Field-Programmable Custom Computing Machines*. FCCM '16. IEEE. 2016, pp. 21–24. DOI: 10.1109/FCCM.2016.13.

[C6] D. Lee, A. Althoff, **D. Richmond**, and R. Kastner. "A Streaming Clustering Approach using a Heterogeneous System for Big Data Analysis". In: *International Conference on Computer-Aided Design*. ICCAD '17. IEEE/ACM. 2017, pp. 699–706. DOI: 10.1109/ICCAD.2017.8203845.

[C7] B. Cain, Z. Merchant, I. Avendano, **D. Richmond**, and R. Kastner. "PynqCopter-An Open-source FPGA Overlay for UAVs". In: *International Conference on Big Data*. Big Data '18. IEEE. 2018, pp. 2491–2498. DOI: 10.1109/BigData.2018.8622102.

[C8] **D. Richmond**, M. Barrow, and R. Kastner. "Everyone's a Critic: A Tool for Exploring RISC-V Projects". In: *International Conference on Field Programmable Logic and Applications*. FPL '18. IEEE. 2018, pp. 260–2604. DOI: 10.1109/FPL.2018.00052.

[C9] A. Rovinski, C. Zhao, K. Al-Hawaj, P. Gao, S. Xie, C. Torng, S. Davidson, A. Amarnath, L. Vega, B. Veluri, A. Rao, T. Ajayi, J. Puscar, S. Dai, R. Zhao, **D. Richmond**, Z. Zhang, I. Galton, C. Batten, M. Taylor, and R. Dreslinski. "A 1.4 GHz 695 Giga RISC-V Inst/s 496-Core Manycore Processor With Mesh On-Chip Network and an All-Digital Synthesized PLL in 16nm CMOS". In: *Symposium on VLSI Circuits*. VLSI '19. IEEE. 2019, pp. C30–C31. DOI: 10.23919/VLSIC.2019.8778031.

[C10] D. C. Jung, S. Davidson, C. Zhao, **D. Richmond**, and M. B. Taylor. "Ruche Networks: Wire-Maximal, No-Fuss NoCs". In: *International Symposium on Networks-on-Chip*. NOCS '20. IEEE/ACM. 2020, pp. 1–8. DOI: 10.1109/NOCS50636.2020.9241586.

[C11] D. Petrisko, C. Zhao, S. Davidson, P. Gao, **D. Richmond**, and M. B. Taylor. "NoC Symbiosis". In: *International Symposium on Networks-on-Chip*. NOCS '20. IEEE/ACM. 2020, pp. 1–8. DOI: 10.1109/NOCS50636.2020.9241584.

[C12] A. Brahmakshatriya, E. Furst, V. A. Ying, C. Hsu, C. Hong, M. Ruttenberg, Y. Zhang, D. C. Jung, **D. Richmond**, M. B. Taylor, J. Shun, M. Oskin, D. Sanchez, and S. Amarasinghe. "Taming the Zoo: The Unified GraphIt Compiler Framework for Novel Architectures". In: *International Symposium on Computer Architecture*. ISCA '21. ACM. 2021. DOI: 10.1109/ISCA52012.2021.00041.

[C13] C. Drewes, S. Harris, W. Wang, R. Appen, O. Weng, R. Kastner, W. Hunter, C. McCarty, and **D. Richmond**. "A Tunable Dual-Edge Time-to-Digital Converter". In: *International Symposium on Field-Programmable Custom Computing Machines*. FCCM '21. IEEE. 2021, pp. 1–1. DOI: 10.1109/FCCM51124.2021.00040.

[C14] M. Gobulukoglu, C. Drewes, B. Hunter, R. Kastner, and **D. Richmond**. "Classifying Computations on Multi-Tenant FPGAs". In: *International Symposium on Field-Programmable Gate Arrays*. FPGA '21. ACM/SIGDA. 2021, p. 227. DOI: 10.1109/DAC18074.2021.9586098.

[C15] M. Gobulukoglu, C. Drewes, B. Hunter, R. Kastner, and **D. Richmond**. "Classifying Computations on Multi-Tenant FPGAs". In: *Design Automation Conference*. DAC '21. 2021. DOI: 10.1109/DAC18074.2021.9586098.

[C16] L. Cheng*, M. Ruttenberg*, D. C. Jung, **D. Richmond**, M. Taylor, M. Oskin, and C. Batten. "Beyond Static Parallel Loops: Supporting Dynamic Task Parallelism on Manycore Architectures with Software-Manged Scratchpad Memories". In: *Architectural Support for Programming Languages and Operating Systems*. Vol. 3. ASPLOS '23. Vancouver, BC, Canada: Association for Computing Machinery, 2023. DOI: 10.1145/3582016.3582020.

[C17] C. Drewes, O. Weng, K. Ryan, B. Hunter, C. McCarty, R. Kastner, and **D. Richmond**. "Turn on, Tune in, Listen up: Maximizing Side-Channel Recovery in Time-to-Digital Converters". In: *International Symposium on Field Programmable Gate Arrays*. FPGA '23. Monterey, CA, USA: Association for Computing Machinery, 2023, pp. 111–122. DOI: 10.1145/3543622.3573193.

[C18] C. Drewes, O. Weng, A. Meza, A. Althoff, D. Kohlbrenner, R. Kastner, and **D. Richmond**. "Pentimento: Data Remanence in Cloud FPGAs". In: *Proceedings of the 29th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Volume 2*. ASPLOS '24. La Jolla, CA, USA: Association for Computing Machinery, 2024, pp. 862–878. DOI: 10.1145/3620665.3640355.

[C19] D. C. Jung, M. Ruttenberg, P. Gao, S. Davidson, D. Petrisko, K. Li, A. K. Kamath, L. Cheng, S. Xie, P. Pan, Z. Zhao, Z. Yue, B. Veluri, S. Muralitharan, A. Sampson, A. Lumsdaine, Z. Zhang, C. Batten, M. Oskin, **D. Richmond**, and M. B. Taylor. " Scalable, Programmable and Dense: The HammerBlade Open-Source RISC-V Manycore ". In: *2024 ACM/IEEE 51st Annual International Symposium on Computer Architecture (ISCA)*. ISCA '24. Los Alamitos, CA, USA: IEEE Computer Society, July 2024, pp. 770–784. DOI: 10.1109/ISCA59077.2024.00061.

JOURNAL PUBLICATIONS (PEER REVIEWED)

[J1] **D. Richmond**, Q. Zhang, G. Cao, and D. N. Weiss. "Pressureless nanoimprinting of anatase TiO_2 precursor films". In: *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena* 29.2 (2011), p. 5. DOI: 10.1116/1.3562955.

[J2] D. N. Weiss, B. G. Lee, **D. Richmond**, W. Nemeth, Q. Wang, D. A. Keszler, and H. M. Branz. "Diffractive light trapping in crystal-silicon films: experiment and electromagnetic modeling". In: *Applied Optics* 50.29 (2011), pp. 5728–5734. DOI: 10.1364/AO.50.005728.

[J3] M. Jacobsen, **D. Richmond**, M. Hogains, and R. Kastner. "RIFFA 2.1: A Reusable Integration Framework for FPGA Accelerators". In: *Transactions on Reconfigurable Technology and Systems* 8.4 (2015). DOI: 10.1145/2815631.

[J4] T. G. Garrison, **D. Richmond**, P. Naughton, E. Lo, S. Trinh, Z. Barnes, A. Lin, C. Schurgers, R. Kastner, and S. E. Newman. "Tunnel Vision: documenting excavations in three dimensions with Lidar technology". In: *Advances in Archaeological Practice* 4.2 (2016), pp. 192–204. DOI: 10.7183/2326-3768.4.2.192.

[J5] **D. Richmond**, A. Althoff, and R. Kastner. "Synthesizable Higher-Order Functions for C++". In: *Transactions on Computer-Aided Design of Integrated Circuits and Systems* 37.11 (2018), pp. 2835–2844. DOI: 10.1109/TCAD.2018.2857259.

[J6] A. Rovinski, C. Zhao, K. Al-Hawaj, P. Gao, S. Xie, C. Torng, S. Davidson, A. Amarnath, L. Vega, B. Veluri, A. Rao, T. Ajayi, J. Puscar, S. Dai, R. Zhao, **D. Richmond**, Z. Zhang, I. Galton, C. Batten, M. Taylor, and R. Dreslinski. "Evaluating Celerity: A 16nm 695 Giga-RISC-V Instructions/s Manycore Processor with Synthesizable PLL". In: *Solid-State Circuits Letters* 2.12 (2019), pp. 289–292. DOI: 10.1109/LSSC.2019.2953847.

[J7] M. B. Taylor, L. Vega, M. Khazraee, I. Magaki, S. Davidson, and **D. Richmond**. "ASIC Clouds: Specializing the Datacenter for Planet-Scale Applications". In: *Communications of the ACM* 63 (2020), pp. 103–109. DOI: 10.1145/3399734.

[J8] L. Cheng, P. Pan, Z. Zhao, K. Ranjan, J. Weber, P. Ivanov, B. Veluri, S. B. Ehsani, M. Ruttenberg, D. Cheol Jung, **D. Richmond**, M. B. Taylor, Z. Zhang, and C. Batten. "A Tensor Processing Framework for CPU-Manycore Heterogeneous Systems". In: *Transactions on Computer-Aided Design of Integrated Circuits and Systems* 41.6 (2021), pp. 1620–1635. DOI: 10.1109/TCAD.2021.3103825.

[J9] C. Drewes, T. Sheaves, O. Weng, K. Ryan, B. Hunter, C. McCarty, R. Kastner, and **D. Richmond**. "Turn on, Tune in, Listen up: Maximizing Side-Channel Recovery in Cross-Platform Time-to-Digital Converters". In: *ACM Trans. Reconfigurable Technol. Syst.* (June 2024). ISSN: 1936-7406. DOI: 10.1145/3666092.

Technical Reports

[R1] **D. Richmond**, M. Jacobsen, and K. Ryan. *RIFFA 2.2.0 Documentation*. University of California, San Diego. San Diego, California, USA, 2014.

[R2] **D. Richmond**, M. Jacobsen, and K. Ryan. *RIFFA 2.2.1 Documentation*. University of California, San Diego. San Diego, California, USA, 2015.

[R3] S. Trinh, **D. Richmond**, P. Naughton, E. Lo, D. Dantas, D. Meyer, A. Lin, C. Schurgers, R. Kastner, and T. Garrison. *La documentación en 3D de excavaciones y artefactos arqueológicos*. Instituto de Antropología e Historia. Guatemala City, Guatemala, 2015.

[R4] **D. Richmond**, M. Jacobsen, and K. Ryan. *RIFFA 2.2.2 Documentation*. University of California, San Diego. San Diego, California, USA, 2016.

Workshop Papers

[W1] J. Matai, **D. Richmond**, D. Lee, and R. Kastner. *Enabling FPGAs for the Masses*. 2014. DOI: 10.48550/arXiv.1408.5870.

Conference, Workshop, and Center Presentations

[P1] *A FPGA Design for High-Speed Feature Extraction from a Compressed Measurement Stream*. Conference Presentation. IEEE International Conference on Field programmable Logic and Applications, 2013.

[P2] *Tinker: Generating Custom Memory Architectures for Altera's OpenCL Compiler*. Conference Presentation. IEEE International Symposium on Field-Programmable Custom Computing Machines, 2016.

[P3] *Synthesizable Higher-Order Functions for C++*. Conference Presentation. ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis, 2018.

[P4] *Deploying Sensors in the Datacenter*. Workshop Presentation. Workshop on Secure Custom Computing Machines at IEEE International Conference on Field-Programmable Custom Computing Machines, 2019.

[P5] *Platforms (And Usability)*. Workshop Presentation. Fast Start Workshop at International Conference on Field-Programmable Custom Computing Machines, 2019.

[P6] *NoC Symbiosis: 10x More Bandwidth for Network-on-Chips*. Virtual Presentation. Semiconductor Research Corporation, Architectures Driving Applications Center e-Workshop, 2021.

[P7] *Optimizing Architectures with Ruche Networks*. Virtual Presentation. Semiconductor Research Corporation, Architectures Driving Applications Center Liason Meeting, 2021.

Posters

[F1] *Design of an Ultra High-Speed Active 3D Scanner*. Conference Poster. University of California, San Diego Research Expo, 2013.

[F2] *Trellis: A Framework for Heterogeneous Desktop Supercomputers*. Poster. University of California, San Diego Research Expo, 2014.

[F3] *Using Computer Vision to Map Environments for Archeological Documentation*. Poster. University of California, San Diego Research Expo, 2015.

[F4] *Using Efficient Heterogeneous Systems in Smart Cities*. Workshop Poster. NSF Early-Career Investigators (ECI) Workshop on Smart City and Cyber-Physical Systems, 2015.

[F5] *Tinker: Generating Custom Memory Architectures for Altera's OpenCL Compiler*. Conference Poster. IEEE International Symposium on Field-Programmable Custom Computing Machines, 2016.

[F6] *Synthesizable Higher-Order functions for C++*. Conference Poster. ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis, 2018.

[F7] *HammerBlade: Continuous Synthesis of Polymorphic Hardware/Software*. Invited Poster. DARPA Microsystems Technology Office Electronics Resurgence Initiative Summit, Detroit, 2019.

[F8] *A Tunable Dual-Edge Time-to-Digital Converter*. Conference Poster. IEEE International Symposium on Field-Programmable Custom Computing Machines, 2021.

[F9] *Classifying Computations on Multi-Tenant FPGAs*. Conference Poster. ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, 2021.

[F10] *HammerBlade: Overcoming Overspecialization with Software-Defined Hardware*. Invited Poster. DARPA Microsystems Technology Office Electronics Resurgence Initiative Summit, Detroit, 2021.

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[M7] Q. Gautier. *Engineers for Exploration - Maya Archaeology*. https://www.youtube.com/watch?v=Ax6hLmHahLg. Oct. 12, 2016.

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[M9] "CSE Closes out Successful Hiring Season for 2016-2017". In: *U.C. San Diego Computer Science and Engineering Newsletter* (Aug. 18, 2017). https://cse.ucsd.edu/about/news/cse-closes-out-successful-hiring-season-2016-2017.

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